The document and process conversion measures necessary to comply with this revision shall be completed by 22 July 2008.

METRIC

MIL–PRF–31032/2A
w/AMENDMENT 3
23 April 2008
SUPERSEDING
MIL–PRF–31032/2A
w/AMENDMENT 2
31 October 2006

PERFORMANCE SPECIFICATION SHEET

PRINTED WIRING BOARD, RIGID, SINGLE AND DOUBLE LAYER, THERMOSETTING RESIN BASE MATERIAL, WITH OR WITHOUT PLATED–THROUGH HOLES, FOR SOLDERED PART MOUNTING

This specification is approved for use by all Departments and Agencies of the Department of Defense.

The requirements for acquiring the product described herein shall consist of this specification sheet and MIL-PRF-31032.

1. SCOPE

1.1 Scope. This specification covers the generic performance requirements for rigid, single and double sided (1 or 2 conductor layers) printed wiring boards (hereafter designated printed board) with or without plated holes that will use soldering for component/part mounting (see 6.1.1).

1.2 Classification. Printed boards are classified as rigid, type 1 (single sided), or type 2 (double sided), as specified (see 6.2).

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3, 4, or 5 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3, 4, or 5 of this specification, whether or not they are listed.

2.2 Government documents. The following specification forms a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-PRF-31032 - Printed Circuit Board/Printed Wiring Board, General Specification for.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil/ or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

Comments, suggestions, or questions on this document should be addressed to Defense Supply Center, Columbus, ATTN: DSCC-VAC, P.O. Box 3990, Columbus, OH 43218-3990, or emailed to 5998.Documents@dscc.dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at http://assist.daps.dla.mil.

AMSC N/A FSC 5998

2.3 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents are those cited in the solicitation or contract.

ASTM INTERNATIONAL (ASTM)

ASTM B567	–	Standard Test Method for Measurement of Coating Thickness by the Beta Backscatter Method.
ASTM B568	–	Standard Test Method for Measurement of Coating Thickness by X-Ray Spectrometry.

(Application for copies should be addressed to the ASTM International, 100 Barr Harbor Drive, P. O. Box C700, West Conshohocken, PA 19428-2959 or http://www.astm.org.)

IPC - ASSOCIATION CONNECTING ELECTRONICS INDUSTRIES (IPC)

IPC-2221	-	Generic Standard on Printed Board Design.
IPC-2222	-	Sectional Design Standard for Rigid Organic Printed Boards.
IPC-A-600	–	Acceptability of Printed Boards.
IPC-TM-650	-	Test Methods Manual.
J-STD-003	-	Solderability Tests for Printed Boards.

(Application for copies should be addressed to the IPC - Association Connecting Electronics Industry, 3000 Lakeside Drive, Suite 309 S, Bannockburn, IL 60015-1249 or http://www.ipc.org.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

2.4 Order of precedence. In the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Printed board detail requirements. Printed boards delivered under this specification shall be in accordance with the requirements as specified herein, and documented in the printed board procurement documentation.

3.1.1 Conflicting requirements. The order of precedence of conflicting requirements shall be in accordance with MIL-PRF-31032.

3.1.2 Reference to printed board procurement documentation. For the purposes of this specification, when the term "specified" is used without additional reference to a specific location or document, the intended reference shall be to the applicable printed board procurement documentation.

3.2 Qualification. Printed boards furnished under this specification shall be technologies that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturers list before contract award (see 4.2 and 6.3).

3.3 Design (see 3.1 and 6.2). Printed boards shall be of the design specified. Unless otherwise noted herein, if individual design parameters are not specified in the printed board procurement documentation, then the baseline design parameters shall be as specified as follows:

a. Overall printed board design baseline shall be in accordance with IPC-2222, type 1 or type 2, performance class 3.

b. Test coupon design, quantity, placement, and usage shall be in accordance with IPC-2221, performance class 3. Test coupons shall be as specified in the applicable design standard and shall reflect worst case design conditions of the printed boards that they represent.

3.4 Printed board materials. All materials used in the construction of compliant printed boards shall comply with the applicable specifications referenced in the printed board procurement documentation. If materials used in the production of printed boards are not specified, then it is the manufacturer's responsibility to use materials which will meet the performance requirements of this specification sheet. Acceptance or approval of any printed board material shall not be construed as a guarantee of the acceptance of the completed printed board.

3.4.1 Tin finishes. Use of pure tin, as an underplate or final finish, is prohibited both internally and externally. Tin content of printed wiring board finishes or solders shall not exceed 97 percent, by mass. Tin shall be alloyed with a minimum of 3 percent lead, by mass (see 6.5).

3.5 External visual and dimensional requirements. Printed board test specimens (the finished printed boards or supporting test coupons, as applicable) shall conform to the requirements specified in 3.5.1 through 3.5.6.5. IPC-A-600 contains figures, illustrations, and photographs that can aid in the visualization of externally observable accept/reject conditions of test specimens. If a condition is not addressed herein, or specified in the printed board procurement documentation, it shall comply with the class 3 criteria of IPC-A-600.

3.5.1 Base material.

3.5.1.1 Edges of base material. Burrs, chips, delaminations, nicks, haloing, and other penetrations along the base material edges of completed printed boards shall be acceptable provided the defect does not reduce the edge spacing specified by more than 50 percent.

3.5.1.2 Surface imperfections. Surface imperfections (such as cuts, dents, pits, scratches, or exposed reinforcement material fibers) shall be acceptable providing the following conditions are met:

a. The imperfections do not bridge between conductors.

b. The dielectric spacing between the imperfection and a conductor is not reduced below the specified minimum conductor spacing requirements.

3.5.1.3 Subsurface imperfections. Subsurface imperfections (such as blistering, delamination, foreign inclusions, and haloing) shall be acceptable providing the following conditions are met:

a. The imperfections do not bridge more than 25 percent of the distance between conductors or plated-through holes. No more than two percent of the printed board area on each side shall be affected.

b. The imperfections do not reduce conductor or dielectric spacing below the specified minimum requirements.

c. The imperfections do not propagate as a result of testing (such as rework simulation, thermal stress, or thermal shock).

d. The longest dimension of any single imperfection is no greater than 0.80 mm (.032 inch). In non-circuitry areas, the maximum size shall not be greater than 2.00 mm (.079 inch) in the longest dimension or 0.01 percent of the printed board area, maximum.

3.5.2 Conductor pattern.

3.5.2.1 Annular ring, external. The external annular ring shall be as specified. Unless otherwise specified, the external annular ring may have, in isolated areas, a 20 percent reduction of the specified external annular ring due to defects such as pits, dents, nicks, or pinholes.

3.5.2.2 Bonding of conductor to base material and lifted lands. There shall be no peeling or lifting of any land or conductor patterns from the base material. The completed printed board shall not exhibit any lifted land. (NOTE: See 3.6.7 for allowances for the acceptable lifting of terminal pads, i.e. lifted lands, following the thermal stress test, rework simulation, and thermal shock testing.)

3.5.2.3 Conductor imperfections. The conductor pattern shall contain no cracks, splits, or tears. Unless otherwise specified, any combination of edge roughness, nicks, pinholes, cuts, or scratches exposing the base material shall not reduce each conductor width by more than 20 percent of its minimum specified width. There shall be no occurrence of the 20 percent reductions greater than 13.0 mm (.51 inch) or 10 percent of a conductor length, whichever is less.

3.5.2.4 Conductor finish. The conductor finish shall be as specified.

3.5.2.4.1 Coverage. The conductor finish shall completely cover the exposed conductor pattern. Complete coverage does not apply to the vertical conductor edges.

3.5.2.4.2 Thickness (non-destructive). The plating or coating thickness of the conductor finish shall be as specified.

3.5.2.4.3 Whiskers. There shall be no whiskers of solder or other platings on the surface of the conductor pattern.

3.5.2.5 Conductor spacing. Conductor spacing shall be as specified.

3.5.2.6 Conductor thickness (non-destructive). The conductor thickness on printed boards shall be as specified. Unless otherwise specified, the minimum final conductor thickness (metal foil) shall not be reduced by more than 10 percent from the starting metal foil nominal thickness as converted from the area weight of the foil.

3.5.2.7 Conductor width. Conductor width shall be as specified.

3.5.3 Dimensions. The completed printed board shall meet the dimensional requirements specified. The dimensional requirements include items such as cutouts, overall thickness, periphery, and other design features as specified.

3.5.4 Hole pattern accuracy. The size and location of the hole pattern in the printed board shall be as specified.

3.5.5 Lifted lands. The completed printed board shall not exhibit any lifted lands.

3.5.6 Solder resist. Unless otherwise specified, the solder resist conditions below shall apply.

3.5.6.1 Coverage. Solder resist coverage imperfections (such as blisters, skips, and voids) shall be acceptable providing the imperfection meets all of the following:

a. The solder resist imperfection shall not expose two adjacent conductors whose spacing is less than the electrical spacing required for the voltage range and environmental condition specified in the applicable design standard.

b. In areas containing parallel conductors, the solder resist imperfection shall not expose two isolated conductors whose spacing is less than 0.50 mm (.020 inch) unless one of the conductors is a test point or other feature area which is purposely left uncoated for subsequent operations.

c. The exposed conductor shall not be bare copper.

d. The solder resist imperfection does not expose tented via holes.

3.5.6.2 Discoloration. Discoloration of metallic surfaces under the cured solder resist is acceptable.

3.5.6.3 Registration. The solder resist shall be registered to the land or terminal patterns in such a manner as to meet the requirements specified. If no requirements are specified, the following apply:

a. Unless otherwise specified, solder resist shall not encroach onto surface mount lands.

b. Solder resist misregistration onto plated-through component hole lands (plated-through holes to which solder connections are to be made) shall not reduce the external annular ring below the specified minimum requirements.

c. Solder resist shall not encroach into plated-through hole barrels or onto other surface features (such as connector fingers or lands of unsupported holes) to which solder connections will be made.

d. Solder resist is permitted in plated-through holes or vias in which no lead is to be soldered.

e. Test points which are intended for assembly testing shall be free of solder resist unless a partial coverage allowance is specified.

3.5.6.4 Thickness. Solder resist thickness shall be as specified.

3.5.6.5 Solder resist cure. The cured solder resist coating shall not exhibit tackiness, blistering, or delamination.

3.6 Microsection requirements (double sided with plated holes only). Printed board test specimens (production printed boards or test coupons) shall conform to the requirements in 3.6.1 through 3.6.7, as applicable (see figure 1). IPC-A-600 contains figures, illustrations, and photographs that can aid in the visualization of internally observable accept/reject conditions of microsectioned test specimens. If a condition is not addressed herein, or specified on the printed board procurement documentation, it shall comply with the class 3 criteria of IPC-A-600.

3.6.1 Conductor finish thickness (plating or coating). The plating or coating thickness of the conductor finish shall be as specified.

3.6.2 Conductor thickness (double sided with plating). The conductor thickness on printed boards shall be as specified. When a conductor thickness is specified, the external conductor thickness (copper foil and copper plating) shall be equal to, or greater than, the specified thickness. When a conductor thickness with tolerance is specified, the external conductor thickness shall be within the specified tolerance for the specified thickness. If only a starting metal foil weight is specified, the limits for external conductors with plating defined in the “external conductor thickness after plating” table of IPC-2221 shall apply.

3.6.3 Plated-through hole plating. Unless otherwise specified, copper plating thickness applies to the hole wall, the hole knee, and the surface land of the plated-through hole.

3.6.3.1 Copper plating thickness. Unless otherwise specified, the copper plating thickness shall be in accordance with the applicable design standard. Any copper plating thickness less than 80 percent of the specified thickness shall be treated as a void.

3.6.3.1.1 Copper plating voids. The copper plating in the plated-through hole shall not exhibit any void in excess of the following:

a. There shall be no more than one plating void for each panel, regardless of length or size.

b. There shall be no plating void longer than five percent of the total printed board thickness.

Conductor finish plating or coating material between the base material and copper plating (i.e., behind the hole wall copper plating) is evidence of a void. Any plated-through hole exhibiting this condition shall be counted as having one void for panel acceptance purposes.

3.6.3.2 Copper plating defects. Nodules, plating folds, plating inclusions, or plated reinforcement material protrusions that project into the plated-through hole shall be acceptable provided that the hole diameter and the copper thickness are not reduced below their specified limits.

3.6.3.3 Wicking. Wicking of copper plating extending 0.08 mm (.003 inch) into the base material shall be acceptable provided it does not reduce the conductor spacing below the minimum clearance spacing requirements specified.

3.6.3.4 Conductive interface separations. Except for along the vertical edge of the external copper foil, there shall be no separations or contamination between the hole wall conductive interfaces. Conductive interface separations along the vertical edge of the external copper foil shall be acceptable. Anomalies resulting from this separation shall not be cause for rejection.

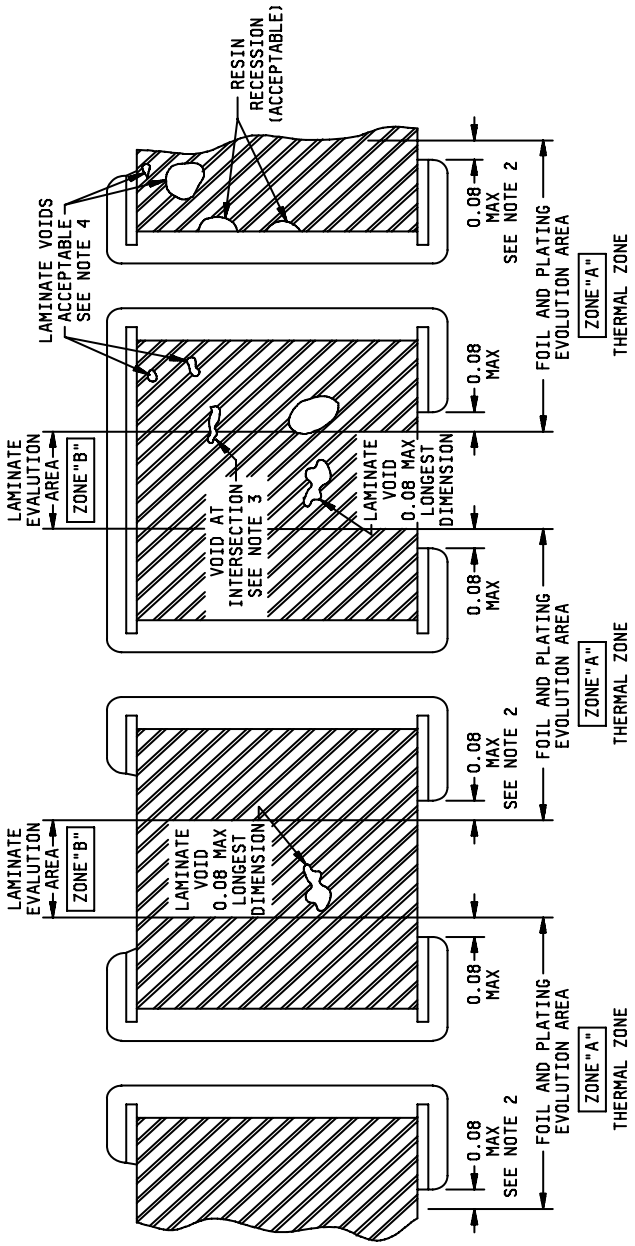
NOTE: The term conductive interfaces shall be used to describe the junction between the hole wall plating or coating and the surfaces of internal and external layers of copper or metal foil. The interface between platings and coating (electroless copper, direct metallization copper, and non-electroless electroless copper substitutes, as applicable, and electrolytic copper, whether panel or pattern plated), shall also be considered a conductive interface.

3.6.4 Metallic cracks. There shall be no cracks in the platings or coatings. For terminal or land areas plated with copper, cracks are permissible in the external layer (outer) copper foil provided they do not extend or propagate into the plated copper.

3.6.5 Dielectric layer thickness. The minimum dielectric thickness between conductor layers shall be as specified.

3.6.6 Laminate voids. Laminate voids with the longest dimension of 0.08 mm (.003 inch) or less shall be acceptable provided the conductor spacing is not reduced below the minimum dielectric spacing requirements, laterally or vertically, as specified. For type 2 designs, after undergoing rework simulation (see 3.7.4.5), thermal stress (see 3.7.6.2), or thermal shock (see 3.7.6.3), laminate voids are not evaluated in zone A (see figure 1).

3.6.7 Lifted lands (after thermal stress, rework simulation, or thermal shock). After undergoing rework simulation (see 3.7.4.5), thermal stress (see 3.7.6.2), or thermal shock (see 3.7.6.3), the maximum allowed lifted land distance from the printed board surface plane to the outer lower edge of the land shall be the thickness (height) of the terminal area or land. The completed, non-stressed printed board shall not exhibit any lifted lands.



NOTES:
1. Dimensions are in millimeters.
2. Typically beyond land edge most radially extended.
3. Voids at intersection of zone A and zone B. Laminate voids greater than 0.08 (.003 inch) that extend into zone B are rejectable.
4. Laminate voids are not evaluated in zone A.

FIGURE 1. Typical plated-through hole cross section after thermal stress or rework simulation.

3.7 Performance requirements. The performance requirements specified in 3.7.1 through 3.7.6.3 shall be verified by the test methods detailed in 4.7. Unless otherwise specified by the Technical Review Board (TRB), test optimization in accordance with MIL-PRF-31032 may be used, but the printed boards shall meet all of the performance requirements specified and herein, regardless of the verification method used.

3.7.1 Acceptability (of printed boards). When examined as specified in 4.7.1, the printed boards shall be in accordance with the acceptance requirements specified in 3.3 (design), 3.4 (material), 3.5 (external visual and dimensional), 3.8 (marking), and 3.9 (workmanship).

3.7.2 Microsection evaluation (of printed board test specimens). When printed board test specimens (completed printed boards, supporting test coupons, or qualification test specimens) are microsectioned and examined as specified in 4.7.2, the requirements specified in 3.1, 3.3, and 3.6 shall be met. Non-stressed microsections shall be evaluated when examination of the stressed microsections suggest that a failure condition may exist in the completed boards (prior to thermal stress).

3.7.3 Chemical requirements.

3.7.3.1 Ionic contamination (cleanliness). When printed board test specimens are tested in accordance with 4.7.3.1, the levels of ionic contamination shall be in accordance with the requirements of 3.7.3.1.1 or 3.7.3.1.2, as applicable.

3.7.3.1.1 Prior to the application of solder resist. Unless otherwise specified, prior to the application of solder resist, the level of ionic contamination shall not exceed 1.56 micrograms/square centimeter (10.06 micrograms/square inch).

3.7.3.1.2 Completed printed boards (when specified, see 3.1 and 6.2.1.a). The levels of cleanliness for completed printed boards shall be as specified.

3.7.3.2 Copper plating characteristics.

3.7.3.2.1 Elongation. When copper plating is tested in accordance with 4.7.3.2, the elongation shall be 12 percent minimum.

3.7.3.2.2 Tensile strength. When copper plating is tested in accordance with 4.7.3.3, the tensile strength shall be 248 MPa (36,000 psi) minimum.

3.7.4 Physical requirements.

3.7.4.1 Adhesion, marking. After marking is tested in accordance with 4.7.4.1, any specified markings which are missing in whole or in part, faded, shifted (dislodged), or smeared to the extent that it cannot be readily identified or is not legible shall constitute failure. A slight change in the color of ink or paint markings after the test shall be acceptable.

3.7.4.2 Adhesion, plating. When tested as specified in 4.7.4.2, there shall be no part of the conductor pattern or copper plating protective finish (coating or plating) removed from the printed board test specimen except for those related to outgrowth, overhang, or slivers.

3.7.4.3 Adhesion, solder resist (when applicable). When tested as specified in 4.7.4.3, the maximum percentage of cured solder resist lifted from the surface of the base material, conductors, and lands of the coated printed board test specimen shall not exceed the following limits:

a. Bare copper or base material: 0 percent.

b. Non-melting metals (e.g., gold or nickel plating): 5 percent.

c. Melting metals (e.g., tin-lead plating, solder coating, indium, bismuth, and others): 10 percent.

3.7.4.4 Bow and twist. When printed boards are tested as specified in 4.7.4.4, the maximum limit for bow and twist shall be as specified.

3.7.4.5 Rework simulation.

3.7.4.5.1 Unsupported holes. After undergoing the test specified in 4.7.4.5.1, the printed board test specimens with unsupported holes shall withstand 2.27 Kg (5 pounds) pull or 3.45 MPa (500 pounds per square inch), whichever is less.

3.7.4.5.2 Plated holes. After undergoing the test specified in 4.7.4.5.2, the printed board test specimens shall be microsectioned and inspected in accordance with 4.7.2 and the requirements specified in 3.6 shall be met.

3.7.4.6 Solderability (see 6.2.1.b).

3.7.4.6.1 Hole solderability. After undergoing the test specified in 4.7.4.6, the printed board test specimen shall conform to the class 3 acceptance criteria specified in J-STD-003.

3.7.4.6.2 Surface solderability. After undergoing the test specified in 4.7.4.6, the printed board test specimen shall conform to the class 3 acceptance criteria specified in J-STD-003.

3.7.5 Electrical requirements.

3.7.5.1 Continuity (when specified, see 6.2.1.d). When tested in accordance with 4.7.5.1, unless otherwise specified, there shall be no circuit whose resistance exceeds 10 ohms. For referee purposes, 0.5 ohm maximum for each 25.0 mm (.98 inch) of circuit length shall apply.

3.7.5.2 Isolation (when specified, see 6.2.1.d). When tested as specified in 4.7.5.2, the resistance between mutually isolated conductors shall be greater than 2 megohms.

3.7.6 Environmental requirements.

3.7.6.1 Moisture and insulation resistance. When tested as specified in 4.7.6.1, the printed board test specimen shall have a minimum of 500 megohms of resistance between conductors. After the test, the printed board test specimen shall not exhibit blistering, measling, or delamination in excess of that allowed in 3.5.1.

3.7.6.2 Thermal stress.

3.7.6.2.1 Unsupported holes. After undergoing the test specified in 4.7.6.2, the printed board test specimen shall be inspected in accordance with 4.7.1 and not exhibit any cracking or separation of plating or conductors, terminals or lands shall not lift in excess of that allowed in 3.6.7, and blistering or delamination shall not exceed the limits in 3.5.

3.7.6.2.2 Plated holes. After undergoing the test specified in 4.7.6.2, the printed board test specimen shall be inspected in accordance with 4.7.1 and blistering or delamination shall not exceed the limits in 3.5. The printed board test specimen shall then be microsectioned and inspected in accordance with 4.7.2 and shall meet the requirements of 3.1, 3.3, and 3.6.

3.7.6.3 Thermal shock. After undergoing the test specified in 4.7.6.3, the printed board test specimens shall meet the following requirements:

a. Visual inspection: When inspected as specified in 4.7.1, there shall be no evidence of plating cracks, blistering, crazing, or delamination in excess of that allowed in 3.5.

b. Resistance change: The change in resistance between the first high temperature cycle and the last high temperature cycle shall not be more than 10 percent.

c. Microsection (double side with plated hole only): The printed board test specimen shall be microsectioned and inspected in accordance with 4.7.2 and the requirements specified in 3.1, 3.3, and 3.6 shall be met.

3.8 Marking. Marking shall be in accordance with MIL-PRF-31032.

3.9 Workmanship. Printed boards shall be processed in such a manner as to be uniform in quality and shall be free from defects that will affect life, serviceability, or appearance.

4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

a. Qualification inspection (see 4.2).

b. Conformance inspection (see 4.3 and tables I and II).

c. Capability verification inspection (see 4.6).

4.1.1 Sampling and inspection. Sampling and inspection shall be in accordance with MIL-PRF-31032, and as specified herein.

4.1.2 Standard test and inspection conditions. Unless otherwise specified by the applicable test method or procedure, inspections and tests may be performed at ambient conditions.

4.2 Qualification inspection. Unless otherwise specified by the TRB approved qualification test plan, qualification inspection shall be in accordance with MIL-PRF-31032 and as specified herein.

4.2.1 Qualification test vehicles. The qualification test vehicle(s) to be subjected to qualification inspection shall be in accordance with the TRB approved qualification test plan and the applicable qualification test vehicle specification(s).

4.2.1.1 Sample. The number of qualification test vehicle(s) to be subjected to qualification inspection shall be in accordance with TRB approved qualification test plan.

4.2.2 Test routine. The qualification test vehicle(s) shall be subjected to the inspections and tests specified in tables I and II in addition to thermal shock in accordance with 3.7.6.3 and 4.7.6.3.

4.2.3 Qualification by similarity. A production lot may be considered qualified by similarity if the dimensional parameters are within twenty-five percent of those currently qualified and the processing steps used are a set or subset of those processes used for a previous qualified technology. When producing printed board designs that are within the 25 percent dimensional parameter region of a qualified process but exceed the currently qualified process limits, the TRB shall review and approve the new process limits.

4.3 Conformance inspection. Conformance inspection shall be in accordance with MIL-PRF-31032 and shall consist of lot conformance inspection (see 4.4) and periodic conformance inspection (see 4.5).

4.4 Lot conformance inspection. Lot conformance inspection shall be in accordance with MIL-PRF-31032 and table I herein. Panels and printed boards to be delivered in accordance with this specification shall have been subjected to and passed all applicable inspections and tests of table I prior to delivery of product. Lot conformance inspection testing by subgroup or within a subgroup may be performed in any sequence.

4.4.1 Sample inspections. Panels and printed boards to be delivered in accordance with this specification shall have been subjected to and passed all the inspections of table I, subgroups 1, 2, 3, 4, and 5.

4.4.1.1 Sampling. A sample of printed boards (or test coupons that represent the printed boards) shall be randomly selected from each inspection lot.

4.4.1.2 Percent defective allowable (PDA) limits. When 100 percent of a production lot is inspected, either in lieu of sampling or due to rejection of a sample inspection lot, the PDA limits for this 100 percent inspection shall be 50 percent.

TABLE I. Lot conformance inspection.

Inspection	Requirement paragraph	Method paragraph	Specimen to test 1/				Sample plan 2/
			PWB	THM	SMT	MIX	
Subgroup 1							
Thermal stress	3.7.6.2	4.7.6.2		A and B	A and B	A and B	Plan TJ
Subgroup 2							
Acceptability	3.7.1	4.7.1	X				Plan BH 3/
Subgroup 3							
Chemical:							
Ionic contamination	3.7.3.1.1	4.7.3.1	X				Plan BN or TN 4/ 5/
Subgroup 4							
Physical:							
Adhesion, marking	3.7.4.1	4.7.4.1	6/	6/	6/	6/	Plan BH or TJ 5/
Adhesion, plating	3.7.4.2	4.7.4.2	X	C	C	C	Plan BH or TJ 5/ 7/
Adhesion, solder resist	3.7.4.3	4.7.4.3	X	G	T 8/	G 8/	Plan BH or TJ 5/
Bow and twist	3.7.4.4	4.7.4.4	X				Plan BH
Solderability							
Hole	3.7.4.6.1	4.7.4.6		S or A		A or S	See 9/
Surface	3.7.4.6.2	4.7.4.6			C or M	C or M	Plan TJ
Subgroup 5							
Electrical:							
Continuity	3.7.5.1	4.7.5.1	X				Plan BH 10/
Isolation resistance	3.7.5.2	4.7.5.2	X				Plan BH 10/

TABLE I. Lot conformance inspection – Continued.

1/ Test coupons are in accordance with IPC-2221. PWB is a production board; THM is a through-hole mount test coupon; SMT is a surface mount test coupon; MIX is for printed board designs containing both through-hole and surface mount components test coupon.
2/ See MIL-PRF-31032 for C = 0 sampling plans.
3/ Surface imperfections (3.5.1.2) and subsurface imperfections (3.5.1.3) shall be inspected prior to solder resist application.
4/ Inspection shall be performed prior to solder resist application. Additional inspections on completed printed boards may be specified.
5/ Test coupon, production panel, or production printed board, manufacturer option.
6/ See 4.7.4.1 for test specimen description and quantity.
7/ All surface platings or coatings shall be inspected.
8/ Test coupon T shall be used when production printed boards have tented via holes (type 2 only).
9/ When using the "S" test coupon, the number of samples to be tested shall be based on a statistical sample of the inspection panels in the lot. When using the "A" test coupon, the number of samples to be tested shall be based on the same statistical sample of the "S" test coupon, but a multiple of four shall be applied to the resulting sample size.
10/ Type 2 only.

4.5 Periodic conformance inspection. Periodic conformance inspection shall be in accordance with TRB approved periodic conformance inspection plan or table II herein.

TABLE II. Periodic conformance inspection baseline test coverage.

Inspection	Requirement paragraph	Method paragraph	Frequency
Elongation 1/	3.7.3.2.1	4.7.3.2	Monthly
Tensile strength 1/	3.7.3.2.2	4.7.3.3	Monthly
Rework simulation 2/	3.7.4.5	4.7.4.5	Monthly
Moisture and insulation resistance 2/	3.7.6.1	4.7.6.1	Monthly

1/ A minimum of ten test specimens (five lengthwise and five crosswise) shall be inspected.
2/ A minimum of two test specimens for each inspection.

4.6 Capability verification inspection. Capability verification inspection shall be in accordance with the TRB approved capability verification inspection plan. The frequency of this verification shall be as a minimum every 2 years. Each base material type qualified shall be verified. The following tests and inspections should be considered when accomplishing capability verification inspection: thermal shock, rework simulation, and moisture and insulation resistance testing.

4.7 Methods of inspection.

4.7.1 Visual and dimensional inspection.

4.7.1.1 Visual inspection. The visual features of the printed board specimen shall be inspected in accordance with test method number 2.1.8 of IPC-TM-650, except that the magnification shall be 1.75x (3 diopters), minimum.

4.7.1.2 Dimensional inspection. The dimensional features of the printed board test specimen shall be inspected using test method numbers 2.2.1 and 2.2.2 of IPC-TM-650, as applicable. Referee inspection needed to confirm a suspected defect of the printed board test specimen features shall be accomplished at a magnification of up to 30X, as applicable to confirm the suspected defect.

4.7.1.3 Alternate plating and coating measurement techniques. When a conductor surface finish plating or coating thickness is less than 0.001 mm (.00004 inch), the thickness measurements shall be performed in accordance with one of the following procedures:

a. ASTM B567, measurement of thickness by the beta backscatter method.

b. ASTM B568, measurement of thickness by X-ray spectrometry.

4.7.2 Microsection inspection.

4.7.2.1 Microsection preparation. Microsection preparation shall be accomplished by using methods in accordance with either test method number 2.1.1 or 2.1.1.2 of IPC-TM-650. Automatic microsectioning techniques may be used in lieu of IPC-TM-650 methods. The following details shall apply:

a. Number of holes for each specimen. A minimum of at least three plated holes cross sectioned vertically shall be made for each test specimen required. Each side of the three plated holes shall be viewed independently. If more than three plated holes are in a row on a test specimen, as with the A/B coupon design, all plated holes in the row shall be evaluated.

b. Accuracy. The plated holes to be evaluated on each test specimen shall be sectioned, ground, and polished to within ±10 percent of the center of the drilled diameter of the hole.

c. Pre–microetch evaluations. The plated holes shall be evaluated for plating separations prior to microetching.

d. When more than two test specimens are contained in a mount (coupon–stacking or gang mounting), the following shall apply:

(1) The test specimens shall not be in direct contact with any other specimen in the mount. The recommended minimum distance between test specimens in a mount is 0.025 mm (.010 inch).

(2) The traceability requirements of MIL-PRF-31032 shall apply.

4.7.2.2 Microsection examination and inspection. Microsection examination and inspection shall be accomplished in accordance with test method number 2.2.5 of IPC-TM-650 to evaluate characteristics such as dielectric spacing, etchback, plating thickness, foil thickness, and so forth, in plated holes. If more than three plated holes are in a row on a test specimen, all holes in the row shall be evaluated. The following details shall apply:

a. Magnifications. Unless otherwise specified in test method number 2.2.5 of IPC-TM-650, the test specimens shall be inspected at a magnification of 100X ±5 percent. Referee inspections shall be accomplished at a magnification of 200X ±5 percent.

b. Evaluations. The plated holes shall be evaluated for plating separations both prior to and after microetching. Pre and post–microetching evaluations for the criteria of 3.1, 3.3, and 3.6 shall be accomplished at magnifications specified above.

c. Measurements. Measurements shall be averaged from at least three determinations for each side of the plated hole. Isolated thick or thin sections shall not be used for averaging; however, isolated areas of reduced copper thickness shall be measured and evaluated to the copper plating void rejection criteria specified in 3.6.3.1.1.

d. Plating or coatings that are less than 0.001 mm (.00004 inch) in thickness shall not be measured using metallographic techniques. See 4.7.1.3 for alternate measurement techniques.

4.7.3 Chemical test methods.

4.7.3.1 Ionic contamination. The test for ionic contamination shall be performed in accordance with test method number 2.3.25 of IPC-TM-650.

4.7.3.2 Elongation of copper. The test for elongation of copper shall be performed in accordance with test method number 2.4.18.1 of IPC-TM-650. The travel speed of testing shall be 50.0 mm ±1.0 mm (1.97 ±.03 inches) for each minute of test.

4.7.3.3 Tensile strength of copper. The test for tensile strength of copper shall be performed in accordance with test method number 2.4.18.1 of IPC-TM-650. The travel speed of testing shall be 50.0 mm ±1.0 mm (1.97 ±.03 inches) for each minute of test.

4.7.4 Physical test methods.

4.7.4.1 Adhesion, marking. Test specimens which represent all types of marking used on the lot (except etched marking) shall be subjected to the solderability test in 4.7.4.6. The side of the test specimen that is marked shall be placed against the solder. After the test, the test specimen shall be examined in accordance with 4.7.1 and the requirements of 3.7.4.1 shall be met.

4.7.4.2 Adhesion, plating. The test for plating adhesion shall be performed in accordance with test method number 2.4.1 of IPC-TM-650. If overhanging metal break off and adheres to the tape, it is evidence of outgrowth, overhang or slivers, but not of plating adhesion failure.

4.7.4.3 Adhesion, solder resist. The test for solder resist adhesion shall be performed in accordance with test method number 2.4.28.1 of IPC-TM-650.

4.7.4.4 Bow and twist. The tests for bow and twist shall be performed in accordance with test method number 2.4.22 of IPC-TM-650.

4.7.4.5 Rework simulation.

4.7.4.5.1 Single and double sided without plated holes. The rework simulation test shall be performed in accordance with test method number 2.4.21 of IPC-TM-650.

4.7.4.5.2 Double sided with plated holes. The rework simulation test shall be performed in accordance with test method number 2.4.36 of IPC-TM-650.

4.7.4.6 Solderability. The tests for hole or surface solderability shall be performed in accordance with J-STD-003. The default category of coating durability of J-STD-003 is category 2. When required by the procurement documentation, accelerated conditioning for coating durability shall be in accordance with J-STD-003.

4.7.5 Electrical test methods.

4.7.5.1 Continuity. A current shall be passed through each conductor or group of interconnected conductors by applying electrodes on the terminals at each end of the conductor or group of conductors. The current passed through the conductors shall not exceed those specified in the applicable design standard for the smallest conductor in the circuit.

4.7.5.2 Isolation (circuit shorts). A test voltage shall be applied between all common portions of each conductor pattern and all adjacent common portions of each conductor pattern. The test voltage shall be applied between conductor patterns of each layer and the electrically isolated pattern of each adjacent layer (when applicable). For manual testing, the test voltage shall be 200 volts minimum and shall be applied for a minimum of 5 seconds. When automated test equipment is used, the minimum applied test voltage shall be the maximum rated voltage specified. If the maximum rated voltage on the printed board is not specified, the test voltage shall be 40 volts minimum.

4.7.6 Environmental test methods.

4.7.6.1 Moisture and insulation resistance. The test for moisture and insulation resistance shall be performed in accordance with class 3 test conditions of test method number 2.6.3 of IPC-TM-650 using specimen preparation method A. The initial and final insulation resistance shall be greater than, or equal to, 500M ohm when measured at 500 volts (+10, -0 percent) dc.

4.7.6.2 Thermal stress. The test for thermal stress shall be performed in accordance with condition A of test method number 2.6.8 of IPC-TM-650.

4.7.6.3 Thermal shock. The test for thermal shock shall be performed in accordance with test method number 2.6.7.2 of IPC-TM-650 except that the temperature extremes shall be –65 degrees Celsius and +125 degrees Celsius for all base materials and minimum dwell time at each temperature extreme shall be 15 minutes.

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

6.1 Notes. The notes specified in MIL-PRF-31032 are applicable to this specification.

6.1.1 Intended use. This specification sheet was developed for the use of verifying the performance of rigid, woven glass reinforced, thermosetting resin base materials, single and double sided printed wiring boards, with or without plated holes, that will use soldering for component mounting. Printed wiring boards of other base material types or construction styles can be tested or verified to the performance requirements contained in this document, however, the performance parameters of other performance specifications sheets may be more appropriate.

6.2 Acquisition requirements. Acquisition documents should specify the following:

a. Title, number, revision letter, and date of this specification.

b. The specific issue of individual documents referenced (see section 2).

c. Title, number, and date of applicable printed board procurement documentation or drawing. Identification of the originating design activity and, if applicable, the Government approved deviation list for the printed board procurement documentation or drawing.

d. The complete product procurement documentation part or identifying number (see 3.1).

e. The printed wiring board classification (type 1 or 2, see 1.2 and 3.3).

f. Title, number, revision letter (with amendment number when applicable), and date of the applicable design standard with performance classification.

g. Requirements for delivery of one copy of the quality conformance inspection data pertinent to the product inspection lot to be supplied with each shipment by the QML manufacturer, if applicable.

h. Requirements for certificate of compliance, if applicable.

i. Requirements for notification of change of product or process to the contracting activity in addition to notification to the qualifying activity, if applicable.

j. Packaging required (see 5.1).

k. If special or additional identification marking is required (see 3.8).

6.2.1 Optional acquisition data. The following items are optional and are only applicable when specified in the printed board procurement documentation.

a. If any special or additional cleanliness is required (see 3.7.3.1.2).

b. The durability of coating rating (accelerated aging for solderability testing) if other than category 2 (see J-STD-003).

c. Requirements for failure analysis, corrective action and reporting of results.

d. If electrical testing is to be performed (see 3.7.5).

e. Disposition of lot conformance inspection sample units.

f. Any other special requirements.

6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QML 31032) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from Defense Supply Center, Columbus, ATTN: DSCC/VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail 5998.Qualifications@dscc.dla.mil or at URL http://www.dscc.dla.mil/offices/sourcing_and_qualification/.

6.4 Replacement information. This specification includes a majority of the performance requirements of previous revisions of MIL-P-55110 and MIL-PRF-55110 for types 1 and 2 printed wiring boards constructed using woven glass reinforced epoxy or polyimide resin base material (legacy types GB, GE, GF, GH, GM, and GI). Printed wiring boards conforming to this associated specification would be comparable to printed wiring boards conforming to MIL-P-55110 or MIL-PRF-55110.

6.5 Tin finishes and whisker growth. Use of tin plating or coating is prohibited (see 3.4.1). The use of alloys with tin content greater than 97 percent, by mass, may exhibit tin whisker growth problems after manufacture. Tin whiskers may occur anytime from a day to years after manufacture and can develop under typical operating conditions on products that use such materials. Conformal coatings applied over top of a whisker-prone surface will not prevent the formation of tin whiskers. Alloys of 3 percent lead, by mass, have shown to inhibit the growth of tin whiskers. For additional information on this matter, refer to ASTM B545 (Standard Specification for Electrodeposited Coating of Tin).

6.6 Amendment notations. The margins of this specification are marked with vertical lines to indicate modifications generated by this amendment. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations.

Custodians:
Army – CR
Navy – EC
Air Force – 11
DLA – CC

Review activities:
Army – MI
Navy – CG
Air Force – 99

Preparing activity:
DLA – CC

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NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at http://assist.daps.dla.mil.